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EXAMINER	
RAHMAN, FAHMIDA	
ART UNIT	PAPER NUMBER
2116	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/699,909	CULLER, JASON HAROLD	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-15,18,20-28,30-35,37 and 38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11, 13-15, 18, 20-28, 30-35, 37-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/30/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to communications filed on 10/30/2007.

2. Claims 1, 13, 15, 25, 30 have been amended, and claims 12, 16-17, 19, 29, 36 have been cancelled. Thus, claims 1-11, 13-15, 18, 20-28, 30-35, 37-38 are pending.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double

patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 2, 13, 14, 15, 25, 26, 30, 37 and 38 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-27 of U.S. Patent No. 7046057, in view of Bi et al (US Patent Application Publication 2003/0052662). Although the conflicting claims are not identical, they are not patentably distinct from each other because, similar to the claimed invention 1 of instant application, the claimed invention in the Patent disclosed a system comprising a sample network that provides plural samples of an delayed input signal (claim 6), detector that provides indication of frequency of the input signal based on samples of input signal state (claim 6), comparator providing comparator signal based on frequency of input signal and a value of desired frequency (claim 10), and a controller operative to implement adjustments to a clock signal based on the comparator signal (claim 10). Although the patent does not claim determining the frequency of the input signal based on the known amount of time, Bi teaches these limitations. Therefore, the above mentioned claims of the pending application are obvious over claims 1-27 of U.S. Patent No. 7046057, in view of Bi et al.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 30-35 and 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Majos (US Patent 6701445).

For claim 30, Majos teaches a method comprising:

- **sampling** (1 in Fig 1) **a signal** (H in Fig 1) **at predetermined and spaced apart time intervals** (H is sampled for each transition of the incoming data signal Din; lines 15-17 of column 5; Q1 and Q3 are apart by dt) **to provide a plurality of output samples indicative of signal state for different time instances of the signal** (Q1, Q2, Q3, Q4 are plural samples);
- **determining a frequency value** (H+, H-) **for the signal based on (i) the output samples received at a detector** (3) **that correspond to time instances of the signal residing within a single period of the signal** (dt can be atmost half period of H. Thus, Q1 and Q3 resides within one period of H), **and (ii) the predetermined and spaced apart time intervals** (Q1 is sampled when Din

transitions and Q3 is sampled after dt interval. 3 detects frequency value H+ and H- based on Q1, Q3);

- **controlling an oscillator** (VCO in Fig 1) **to provide the signal at a frequency based on a comparison of the frequency value for the signal relative to a desired frequency value** (4 performs a comparison between desired HE and H+/H-).

For claims 31, 32 and 35, 14-17 are the storage elements and clock edges are provided to storage elements.

For claim 33, 12 delays the clock to provide the clock edges.

For claim 34, dt is known. H is delayed by dt in 16 to establish time intervals such as transition in Din and dt+ transition in Din.

For claim 37, oscillator does not change when H+, H- is 00.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 9, 11, 13, 14, 25, 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Majos (US Patent 6701445).

For claim 1, Majos teach the following limitations:

A system comprising:

a sample network (1) **that provides plural samples** (Q1, Q2, Q3, Q4) **of an input signal state** (1H) **for different time instances of the input signal** (H is sampled for each transition of the incoming data signal Din; lines 15-17 of column 5; Q1 and Q3 are apart by dt), **each of the plural samples corresponding to the input signal delayed by a known amount of time** (Q1 is delayed by "0" corresponding to input signal H when Din transitions and Q3 is delayed by dt corresponding to input H when Din transitions); **and a detector** (3) **that determines the frequency for the input signal** (H+, H-) **based on samples of the input signal state received by the detector for different time instances of the input signal residing within one period of the input signal** (dt can be atmost half period of H. Thus, Q1 and Q3 resides within one period of H), **and the known amount of time for each of the plural samples** ("0" delay and "dt" delay is known), **the detector provides a value that represents the frequency of the input signal** (H+, H- represents frequency of H with respect to Din. For example, when H+, H- is 00, H and Din are substantially at the same frequency); **a comparator** (4) **that provides a comparator signal based on a comparison of the value of the frequency for the input signal** (4 compares between H+H- with HE) **and a value of a desired frequency** (HE represents the desired frequency because HE is derived from

Din and the goal is to make H having mean clock frequency of Din); **and a controller** (5 and 6) **operative to implement adjustments to a clock signal based on the comparator signal** (H is adjusted according to lines 50-51 of column 4).

However, detector 3 provides a value that represents an indication of frequency, or a frequency value, not the determined frequency as recited in claim 1. Table shown in column 7 mentions that H+H- = 00 means H and Din are at substantially same frequency (lines 15-20 of column 7).

Majos provides second embodiment where Din is a known frequency (Fig 5 shows Hr as Din. Lines 10-42 of column 11 mention that how Hr can be programmed). Thus, when H is equal to Hr, the frequency of H is determined and known, which is provided by the detector as H+H- = 00).

For claims 2, 9, 11, 14-17 are the storage elements.

For claim 13, oscillator VCO generates clock signal H.

For claim 14, Majos does not explicitly mention about IC chip. Examiner takes an official notice that the system implemented within the IC chip is well known in the art. An ordinary skill in the art would have been motivated to implement the system within the IC chip for many reasons, such as, to make commercially available to the customers.

For claim 25, Majos teaches the following limitations:

A frequency detection system comprising:

means for sampling (1) **an input signal** (H) **having an unknown frequency and for providing plural indications of signal state** (Q1, Q2, Q3, Q4) **associated with different time instances of the input signal** (H is sampled for each transition of the incoming data signal Din; lines 15-17 of column 5; Q1 and Q3 are apart by dt) **delayed for different amounts of time** (Q1 is delayed by "0" corresponding to input signal H when Din transitions and Q3 is delayed by dt corresponding to input H when Din transitions); **and means for determining a frequency** (3) **for the input signal based on I) the plural indications of signal state received by the means for determining, that correspond to time instances of the input signal residing within a single period of the input signal** (dt can be atmost half period of H. Thus, Q1 and Q3 resides within one period of H) **and ii) the known amounts of time** ("0" delay and "dt" delay is known); **and means for providing a corresponding frequency value for the determined frequency** (H+, H- represents frequency of H with respect to Din. For example, when H+, H- is 00, H and Din are substantially at the same frequency);

means for comparing (4) **the frequency value** (4 compares between H+H- with HE) **relative to a desired frequency value** (HE represents the desired frequency because HE is derived from Din and the goal is to make H having mean clock frequency of Din); **and means for controlling the frequency of the input signal based on the**

comparison of the frequency of the input signal and the desired frequency (H is adjusted according to lines 50-51 of column 4).

However, detector 3 provides a value that represents an indication of frequency, or a frequency value, not the determined frequency as recited in claim 1. Table shown in column 7 mentions that H+H- = 00 means H and Din are at substantially same frequency (lines 15-20 of column 7).

Majos provides second embodiment where Din is a known frequency (Fig 5 shows Hr as Din. Lines 10-42 of column 11 mention that how Hr can be programmed). Thus, when H is equal to Hr, the frequency of H is determined and known, which is provided by the detector as H+H- = 00).

For claim 26, delaying means are selected parts of sampling means.

For claims 27 and 28, Fig 2 shows the storage elements and delaying the clock signal to provide the activation signal.

5. Claims 3-8, 10, 15, 18, 20-24, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Majos, in view of Lee et al (US Patent 6326826).

For claim 3, Majos does not teach plurality of delay elements providing respective delayed clock signals to clock the storage elements. Lee et al teach plural storage

elements (22') to provide samples (EDGE[N]) corresponding to plural samples of REF_CK at the output of delay elements. The system of Lee et al further comprises delay elements (Delay0-Delay6) for delayed clock signal (CK[N]) to clock storage 22' to sample input signal at different time interval (the plural samples of input signal just at the end of delay elements are sampled at different time interval) and thereby providing plural samples of the input signal state to the decision logic 23.

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Majos and Lee et al. One ordinary skill would be motivated to use storage elements with delay elements when sequential design is desirable.

For claim 4, input signal REF_CK of Lee is delayed by delay elements.

For claims 5 and 6, clock signal activates the storage elements in Fig 2 of Lee. However, neither Bi nor Lee teaches that the oscillator generates the clock signal that is activating the storage.

Examiner takes an official notice that the oscillator generating clock signal is well known in the art. An ordinary skill in the art would have been motivated to have an oscillator providing the clock signal REF_CK, since oscillator provides an on-chip generation of

clock signal. The oscillator generated signal is divided by PLL and therefore, oscillator generated clock typically has higher frequency that the supplied clock.

For claim 7, Lee et al teach 7 storage elements (22') to provide samples (EDGE[N]) corresponding to plural samples of REF_CK at the output of 7 delay elements. The system of Lee et al further comprises delay elements (Delay0-Delay6) with fixed known amount of delay for delayed clock signal (CK[N]) to clock storage 22' to sample input signal at different time interval (the plural samples of input signal just at the end of delay elements are sampled at different time interval) and thereby providing plural samples of the input signal state to the decision logic 23.

For claim 8, delay components are in series. The oscillator can be used to generate a clock from which REF_CK can be generated.

For claim 10, H is a direct input to 14 and 16.

For claim 15, Majos teaches the following:

A system comprising:

a plurality of storage elements (14, 15, 16, 17 of Fig 2), **the plurality of storage elements being clocked to latch** (Fig 2) **different time instances of an input signal** (1H in Fig 2) **to provide corresponding output samples of the input signal** (Q1(Tn),

Q2 (Tn-k), Q3(Tn+dt), Q4(Tn-k+dt) of Fig 2) **sufficient for determining a frequency value** (H+, H-) **of the input signal** (3 determines frequency value H+, H- from Q1-Q4); **a plurality of delay elements** (output of 10 goes to delay 12 and "0" delay path 10 to 14, which can be thought as a delay element with "0" delay) **associated with at least a substantial number of the storage elements** (11-12 are associated with 14-17), **each of the delay elements delaying a sample signal** (output of 10) **by a respective known amount of time** (delayed by "0" and delayed by "dt") **to provide a respective clock signal** (Fig 2) **that clocks a respective one of the at least a substantial number of the storage elements** (clock signals clock 14-17 in Fig 2) **to latch a respective one of the different time instances of the input signal** (the different instances of input signal is latched as shown in Fig 2) **to provide at least a portion of the corresponding output samples** (Fig 2); **and a detector** (3) **that provides a frequency value** (H+, H-) **for the input signal** (combination of H+, H- is a frequency value for the input signal as the combination provides indication of frequency of H as explained in table of column 7) **based (i) on output samples that correspond to different time instances of the input signal** (Q1-Q4 are input to 3 as shown in Fig 1) **and (ii) the known amount of time for each respective delay element** (samples are dependent on the "0" delay and "dt" delay and 3 provides frequency value based on samples, the detector provides frequency value based on output samples and the known amount of time).

Although the "0" delay path 10 to 14 can be thought as a delay element, Examiner cites Lee to provide a better explanation. Lee teaches delay elements delaying sample signal. Therefore, one ordinary skill may put one more delay element in the path of 10 to 14 for a different design. Such a modification is possible within the scope of Majos and can provide better sampling of H.

For claim 18, Majos teaches the plurality of delay elements to provide the respective delayed clock signals (clock to 14-15 has 0 delay, clock to 16-17 has dt delay) for clocking the at least a substantial number of the storage elements to latch the different time instances of the input signal into the storage elements (Fig 2). Majos does not teach that the input signal comprises the sample signal and the input signal being delayed by the plurality of delay elements.

Lee et al teach input signal comprises sample signal, the input signal delayed by delay elements (Fig 1).

It would have been obvious for one ordinary skill in the art to combine the teachings of Majos and Lee. One ordinary skill would be motivated to have the input signal comprises the delay signal depending on his design criterion.

For claim 20, lines 60-62 of Majos mention that sample signal is a clock signal. However, it does not mention oscillator.

Examiner takes an official notice that the oscillator generating clock signal is well known in the art. An ordinary skill in the art would have been motivated to have an oscillator providing the clock signal, since oscillator provides an on-chip generation of clock signal.

For claim 21, Lee et al teach that the delay elements (18') provide respective clock edges (CK[1:7] in Fig 2) for activating the storage elements (22'), each of the clock edges corresponding to a different delayed version of the clock signal (11).

For claim 22, the delay elements in 11 of Lee et al are connected in series.

For claim 23, Majos teaches that the input H is directly connected to the plurality of storage.

For claim 24, 14-15 of Majos are clocked at an interval "0" and 16-17 are clocked at interval "dt" to latch the output samples to the detector concurrently.

For claim 38, H+ and H- are not expressed in unit of inverse of period. The second embodiment mentions that Fr can be expressed as unit of Hz. As H+H- = 00 implies Fr and H is at equal frequency, it is possible for one ordinary skill to express the frequency value in unit of Hz.

Response to Arguments

Applicant's arguments with respect to claim 1-11, 13-15, 18, 20-28, 30-35, 37-38 have been considered but are moot in view of the new ground(s) of rejection. As Majos is still relied upon for rejections, Examiner is addressing the arguments regarding Majos.

Applicant argues that Q1-Q4 inputs do not correspond to frequency of input signal and desired frequency. The comparator does not compare desired frequency and frequency of input signal.

Examiner disagrees. H+H- represents the frequency of input signal and HE represents the desired frequency. 4 performs a comparison and outputs a signal to adjust H (lines 15-35 of column 8). HE represents the desired frequency as HE is derived from Din, and the goal is to have H with a mean frequency of Din (lines 50-51 of column 4).

Applicant further argues that XOR gate or the delay line 12 does not provide delayed versions of sample signal because output of 10 is not delayed version of Din.

Examiner agrees that output of 10 is not delayed version of Din. However, output of 10 is the sample signal, which is delayed by "0" and delayed by "dt". "0" delay can be considered as a delay element. Besides Lee clearly shows that plural delay elements.

Applicant further argues that Majos fails to include the delay elements in a path from the oscillator to the storage elements.

Examiner cited Lee for plural delay elements. The delay element can be put after 10 and before 12 in Majos. Then the delay corresponds to number of delay elements from oscillator to storage elements.

Applicant further argues that expressing frequency value in units of inverse of a period of an input signal is not obvious for Majos.

Examiner disagrees. The second embodiment in Majos shows that the reference frequency can be determined in Hz (lines 30-35 of column 11). As in some instances, H is equal to reference frequency (H+H- = 00), the frequency of input signal can be expressed in Hz at least for some instances.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116

A. ELAMIN
PRIMARY EXAMINER